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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,010	07/22/2003	Kevin Weaver	100-22400 (PO5620)	8431

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LAW OFFICES OF MARK C. PICKERING
P.O. BOX 300
PETALUMA, CA 94953

EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 06/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/625,010	WEAVER ET AL.
	Examiner	Art Unit
	Tu-Tu Ho	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-10,19,20,23,25 and 28-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-10,19,20,23,25 and 29-34* is/are rejected.

7)☒ Claim(s) *28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 August 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "adhesive" of **claim 3** must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Allowable Subject Matter

2. The indicated allowability of claims 2-10, 19-20, 23, 25, and 29-34 is withdrawn in view of the newly discovered reference(s) to Akram et al. U.S. Patent 6,022,750, Farnworth et al. U.S. Patent Application Publication 20030106209, Kishimoto et al. U.S. Patent Application Publication 20010048980, Lin U.S. Patent Application Publication 20020105076. Rejections based on the newly cited reference(s) follow.

Claim Rejections § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

A. As a matter of providing proofs and definitions of certain terminologies used in the art and in the rejection, the following are cited first:

a. A die is a semiconductor integrated circuit device that does not necessarily include a bond pad or a contact pad. For example, Farnworth et al. U.S. Patent Application Publication 20030106209 (the '209 reference), who teach in Fig. 5 a die 92 and a bondpad 120 on a top surface of the die (paragraph [0069]: "bond pads 120 (or other contact locations) on the die 92"). In other words, a bondpad might be considered separated from the die.

b. At the time the invention was made, a semiconductor device should comprise multilevel interconnections and inter-layer insulators to increase density (KISHIMOTO et al. U.S. Patent Application Publication 20010048980, paragraph [0002]).

c. A semiconductor die including a multilevel interconnection structure comprises - as an example, Fig. 1, paragraphs [0005]-[0006] by Downey et al. U.S. Patent Application Publication 20040036174 - a semiconductor structure that includes a plurality of device regions

("active circuitry") formed in and over a substrate 19, the device region being conductive, and an interconnect structure 20 that contacts the semiconductor structure, and forms a top surface of the die, the interconnect structure including a dielectric structure 20 and a plurality of layers of metal (21,22,23) that are formed in and isolated by the dielectric structure, each metal layer having a plurality of metal traces that are electrically connected to the device regions.

3. **Claims 23, 25, and 29-32** are rejected under 35 U.S.C. 103(a) as obvious over Akram et al. U.S. Patent 6,022,750 (the '750 reference) in view of KISHIMOTO et al. U.S. Patent Application Publication 20010048980 (the '980 reference).

The '750 reference discloses in Figs. 2-14 and respective portions of the specification a semiconductor device substantially as claimed.

Referring to **claim 23**, the reference discloses a semiconductor device comprising:

a die (12, column 4, first paragraph); and

a test structure (16, Figs. 2-4) that contacts a top surface of the die, the test structure including a capacitor (80 or 82, column 5, first paragraph).

However, the '750 reference does not disclose structural details of the die 12. The reference further fails to disclose that the die comprises a multilevel interconnect structure as claimed.

Nevertheless, KISHIMOTO, in disclosing also a semiconductor die, as noted above in section A-b, teaches that a semiconductor die should comprise multilevel interconnections and inter-layer insulators to increase density.

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the reference's die with a multilevel interconnections. One would have been motivated to make such a change because a die including a multilevel interconnection structure has increased density.

A die such modified would comprise all limitations as detailed above in section A-c, and the modified die would comprise:

a first opening formed in the dielectric structure (such as 20, the Downey reference) of the die, the first opening extending from the top surface down to a first region on a metal interconnect (such as 21,22,23); and

a first conductive structure formed in the first opening to make an electrical contact with the first region, and on the top surface to make an electrical contact with the test structure (so as the capacitor test structure of the '750 reference makes an electrical contact with the first region).

Referring to **claim 25**, in order for the capacitor test structure, which comprises two terminals, to function, a second opening should be formed in the dielectric structure to reach a second region of the metal interconnect, and a second conductive structure formed in the second opening to make an electrical contact with the second region, and on the top surface to make an electrical contact with the test structure.

Referring to **claim 29**, the reference discloses a semiconductor device comprising:

a die (12, column 4, first paragraph); and

a test device (16) formed on an exterior surface of the die (and note that the structure of Fig. 4 is or could be turned upside down), the test device including a region (60 and/or 64) of silicon (column 4, lines 52-58).

However, the '750 reference does not disclose structural details of the die 12. The reference further fails to disclose that the die comprises a multilevel interconnect structure as claimed.

Nevertheless, KISHIMOTO, in disclosing also a semiconductor die, as noted above in section A-b, teaches that a semiconductor die should comprise multilevel interconnections and inter-layer insulators to increase density.

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the reference's die with a multilevel interconnections. One would have been motivated to make such a change because a die including a multilevel interconnection structure has increased density.

In reference to **claim 30**, a die such modified would comprise all limitations as detailed above in section A-c, and the modified die would comprise:

a first via that is electrically connected to a device region and a first end of the test device (for the test structure to function);

and a second via that is electrically connected to a device region and a second end of the test device (for the multiple-point test structures depicted in Figs. 5-14 to function).

Referring to **claim 32**, the reference further discloses:

a dielectric region ("insulating layer" 66, Fig. 4, column 4, lines 52-60) formed to contact the region (60) of silicon; and

a conductor region (68) formed to contact the dielectric region.

4. **Claims 2, 4, 9-10, 19, and 29-30** are rejected under 35 U.S.C. 103(a) as obvious over Farnworth et al. U.S. Patent Application Publication 20030106209 (the '209 reference) in view of KISHIMOTO et al. U.S. Patent Application Publication 20010048980 (the '980 reference).

The '209 reference discloses in Figs. 4-5 and respective portions of the specification a semiconductor device substantially as claimed.

Referring to **claims 2 and 19**, the reference discloses a semiconductor device comprising:

a die (92, paragraph [0069]); and

a conductive region (118a, Fig. 5) formed over the top surface of the die (and note that the structure of Fig. 5 is or could be turned upside down), the conductive region including silicon (paragraph [0067], which is non-metallic).

However, the '209 reference does not disclose structural details of the die 92. The reference further fails to disclose that the die comprises a multilevel interconnect structure as claimed.

Nevertheless, KISHIMOTO, in disclosing also a semiconductor die, as noted above in section A-b, teaches that a semiconductor die should comprise multilevel interconnections and inter-layer insulators to increase density.

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the reference's die with a multilevel interconnection structure. One would have been motivated to make such a change because a die including a multilevel interconnection structure has increased density.

A die such modified would comprise all limitations as detailed above in section A-c, and the modified die would comprise a plurality of layers of metal (such as 21,22,23, the Downey

reference), and the conductive region 118a of the '209 reference would be above the plurality of layers of metal.

Referring to **claim 29**, the reference discloses a semiconductor device comprising:

a die (92, paragraph [0069]); and

a test device (119, Fig. 4B) formed on an exterior surface of the die (and note that the structure of Fig. 4B is or could be turned upside down), the test device including a region (118a or 119a) of silicon (paragraph [0067]).

However, the '209 reference does not disclose structural details of the die 92. The reference further fails to disclose that the die comprises a multilevel interconnect structure as claimed.

Nevertheless, KISHIMOTO, in disclosing also a semiconductor die, as noted above in section A-b, teaches that a semiconductor die should comprise multilevel interconnections and inter-layer insulators to increase density.

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the reference's die with a multilevel interconnection structure. One would have been motivated to make such a change because a die including a multilevel interconnection structure has increased density.

In reference to **claim 4**, a die such modified would comprise a first via that makes an electrical connection with a region of a metal trace and a first end of the conductive region (of the test structure 119, for the test structure to function) and a second via that makes an electrical connection with a region of a metal trace and a second end of the conductive region (of the test structure 119, for the test structure to function effectively).

In reference to **claim 30**, a die such modified would comprise a first via that is electrically connected to a device region and a first end of the test device (for the test structure to function) and a second via that is electrically connected to a device region and a second end of the test device (for the test structure to function effectively).

Referring to **claim 9**, the dielectric structure of the die of the '209 reference such modified further includes a plurality of layers, including an overlying passivation layer (such as 15, Downey reference), the conductive region being formed over the passivation layer.

Referring to **claim 10**, the semiconductor device of the '209 reference such modified further comprises:

a plurality of contacts (not shown) formed in the dielectric structure, the contacts electrically connecting the device regions to the metal traces (such as generally defined by 21, Downey reference) that are formed from a first layer of metal (21);

a plurality of vias (no number) formed in the dielectric structure, the vias electrically connecting vertically adjacent metal traces and regions; and

a plurality of pads (120, the '209 reference; such as 14, Downey reference) formed in the dielectric structure, the pads being connected to a number of vias to form external points of electrical connection.

5. **Claims 2, 6, and 19-20** are rejected under 35 U.S.C. 103(a) as obvious over Lin U.S. Patent Application Publication 20020105076 (the '076 reference) in view of KISHIMOTO et al. U.S. Patent Application Publication 20010048980 (the '980 reference).

The '076 reference discloses in the figures, particularly Figs. 2-4, and respective portions of the specification a semiconductor device substantially as claimed.

Referring to **claims 2 and 19**, the reference discloses a semiconductor device comprising:

a die (generally defined as 10/13 or 10/29); and

a conductive region (bond pad or contact pad 17 or 14, Fig. 2 or Fig. 4) formed over the top surface of the die, the conductive region including silicon (paragraph [0008], which is non-metallic).

However, the '076 reference does not disclose structural details of the die. The reference further fails to disclose that the die comprises a multilevel interconnect structure as claimed.

Nevertheless, KISHIMOTO, in disclosing also a semiconductor die, as noted above in section A-b, teaches that a semiconductor die should comprise multilevel interconnections and inter-layer insulators to increase density.

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the reference's die with a multilevel interconnection structure. One would have been motivated to make such a change because a die including a multilevel interconnection structure has increased density.

A die such modified would comprise all limitations as detailed above in section A-c, and the modified die would comprise a plurality of layers of metal (such as 21,22,23, the Downey reference), and the conductive region 118a of the '209 reference would be above the plurality of layers of metal.

In reference to **claim 6**, a semiconductor device such modified would further comprise:

a dielectric region (16, Fig. 4) formed to contact the conductive region (14); and

a conductive region (18) formed to contact the dielectric region.

Referring to **claim 20**, the '076 reference further discloses that the conductive region (14 or 17) has a concentration of dopant atoms (paragraph [0008]).

6. **Claims 4-5 and 7-8** are rejected under 35 U.S.C. 103(a) as obvious over Lin U.S. Patent Application Publication 20020105076 (the '076 reference) in view of KISHIMOTO et al. U.S. Patent Application Publication 20010048980 (the '980 reference) as applied above and further in view of Lu et al. U.S. Patent 6,100,573.

Referring to **claims 4 and 7**, the '076 reference and Kishimoto disclose a semiconductor device substantially as claimed and as detailed above for claim 2, including a conductive bond pad region 14 or 17 that is equivalent to the claimed conductive region, and further disclose an inherent via that makes an electrical connection with a region of a metal trace and the conductive region for the device to function, but fail to disclose a second via that makes an electrical connection with a region of a metal trace and the conductive region or a second end of the conductive region.

Lu, in disclosing also a semiconductor device and in particular a conductive bond pad region for a semiconductor device, teaches that a conductive bond pad region, which is the equivalent of the conductive bond pad region 14 or 17 of the '076 reference, which in turn is equivalent the claimed conductive region, comprises multiple layers and vias, thus comprising a second via that makes an electrical connection with a region of un underlying metal trace and the conductive region or a second end of the conductive region, so as to reduce stress therebetween (column 1, lines 50-67).

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the '076/Kishimoto reference's device such that it further includes a second via that makes an electrical connection with a region of a metal trace and the conductive region or a second end of the conductive region. One would have been motivated to make such a change because that additional second via helps reduce stress.

In reference to **claims 5 and 8**, the conductive region (14 or 17) of a semiconductor device such modified further has a concentration of dopant atoms (the '076 reference, paragraph [0008]).

7. **Claim 3** is rejected under 35 U.S.C. 103(a) as obvious over Lin U.S. Patent Application Publication 20020105076 (the '076 reference) in view of KISHIMOTO et al. U.S. Patent Application Publication 20010048980 (the '980 reference) as applied above and further in view of Yin et al. U.S. Patent Application Publication 20030049882.

The '076 reference and Kishimoto disclose a semiconductor device substantially as claimed and as detailed above for claim 2, including a conductive contact pad region 14 or 17 that is equivalent to the claimed conductive region including silicon, but fail to disclose that the silicon, which is the conductive region, which is the silicon conductive bond pad 14 or 17, is attached via an adhesive.

Yin, in disclosing also a semiconductor device and in particular a conductive contact pad region for a semiconductor device, teaches that an intermediate layer (24) promotes adhesion of the outer layer (56), which is the same as the layer 14 or 17 of the '076/Kishimoto reference,

which in turn is equivalent the claimed silicon conductive region, to an underlying layer of the semiconductor device (paragraph [0024]).

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the '076/Kishimoto reference's device such that it further includes another layer functioning as ad adhesion layer. One would have been motivated to make such a change because that another layer promotes adhesion of the layer 14 or 17 of the '076/Kishimoto reference, which is equivalent the claimed silicon conductive region, to an underlying layer of the semiconductor device, which is the die.

8. **Claims 31 and 33-34** is rejected under 35 U.S.C. 103(a) as obvious over Akram et al. U.S. Patent 6,022,750 (the '750 reference) in view of KISHIMOTO et al. U.S. Patent Application Publication 20010048980 (the '980 reference) as applied above and further in view of Akram et al. U.S. Patent 5,419,807 (the '807 reference).

Referring to **claim 33**, Akram in the '750 reference discloses a semiconductor device substantially as claimed and as detailed above for claim 32, including the test device having the region 60 of silicon and the conductive region 68, and further discloses that a first via is electrically connected to a device region and the conductive region and a second via is electrically connected to a device region and the conductive region. In other words, the reference teaches electrical connection to the conductive region only as opposed to the region of silicon and the conductive region.

Akram in the '807 reference, in disclosing also a semiconductor device including a test device having a region of silicon (38, Fig. 6), teaches that an inherent via could be electrically connected to an inherent device region and the region of silicon 38.

The missing limitation is therefore obvious for at least one of the following two reasons: 1) Applicant has not established why it is critical, thus contribute to patentability, to form the claimed device such that a first via is electrically connected to a device region and the region of silicon and a second via is electrically connected to a device region and the conductive region rather than forming the claimed device such that a first via is electrically connected to a device region and the conductive region and a second via is electrically connected to a device region and the conductive region; and 2) as taught by Akram in the '807 reference that a first via could be electrically connected to a device region and the region of silicon, therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the reference's device such that a first via is electrically connected to a device region and the region of silicon and a second via is electrically connected to a device region and the conductive region. One would have been motivated to make such a change simply to be able to choose from the different available known electrical connections.

Referring to **claim 31 and 34,** Akram in the '750 reference discloses a semiconductor device substantially as claimed and as detailed above for claims 30 and 33, including the test device having the region 60 of silicon, but fails to teach that the region of silicon has a concentration of dopant atoms.

Akram in the '807 reference, in disclosing also a semiconductor device including a test device having a region of silicon (12/26, Fig. 4), teaches that the region of silicon has a

concentration of dopant atoms for enhancing conductivity ("conductivity enhancing impurity", column 5, lines 54-60).

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the '750 reference's region of silicon 60 such that the region of silicon 60 has a concentration of dopant atoms. One would have been motivated to make such a change because dopant atoms enhances conductivity, as taught in the '807 reference.

Allowable Subject Matter

9. **Claim 28** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious a semiconductor device having all exclusive limitations as recited in claims 23/25/28 (claims 23, 25 and 28), characterized in the third opening extending through the metal interconnect to break an electrical connection between the first and the second regions of the metal interconnect.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
June 02, 2005